The Declining Drain Line Lengths Circuit—A Computer Derived Design Concept Applied to a 2–26.5-GHz Distributed Amplifier

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Abstract — **The principle of the "declining drain line lengths" has emerged as a successful concept in the pursuit of improved gain flatness and bandwidth. The optimized performance parameters of an "identical links" gain module are compared to those of a "declining drain line lengths" gain module, and the advantages of one design principle over the other are discussed. In addition, the paper studies the RF voltages and currents of the circuits' GaAs MESFETs and draws some qualitative conclusions as to the causes of gain limiting when approaching nonlinear operation. Finally, experimental results of a power module based on the "declining drain line lengths" principle are reported. The hybrid amplifier which incorporates five active devices with 0.25-μm gates achieves a small signal gain of $G = 6.1 \pm 0.6$ dB from 2–27 GHz. Measurements of its output power, reflection coefficients and noise figure are also discussed.**

I. Introduction

THE FEASIBILITY of distributed amplification for multi-octave frequency bands has been convincingly demonstrated in both monolithic and hybrid solid-state amplifiers [1]–[6]. The principle is based on the idea of neutralizing the bandwidth limiting effects of the active devices' parasitic capacitances by making them part of artificial transmission lines that link the active devices. This concept was first demonstrated by W. S. Percival in 1935 [7] but with the development of GaAs MESFETs it is making a dramatic comeback. While some distributed amplifier circuits are employing identical delay line elements on both the gate and the drain side of the transistor and have their idle ports terminated with resistors that match the characteristic impedances of the artificial transmission lines, others deviate from this design method. Modifications range from different lengths and characteristic impedances of the drain versus the gate line to terminations other than those matching the line's characteristic impedances. However, with one exception [8], all cases reported to date make use of identical four-ports between the active devices.

Obviously, a number of options outside the approach of identical links are available to the amplifier designer who not only may be seeking improved performance but also may be restrained by dimensional problems. Since available computer programs provide the means to optimize each circuit element for a desired performance, a new concept using individually optimized links can easily be explored. A design principle that has grown out of our studies is that of the "declining drain line lengths." By comparing the computed performance parameters of an "identical links" gain module with those of a module designed in accordance with the proposed method, certain advantages of one over the other become evident and are discussed in detail. In addition to gain, gain flatness and noise figure, the paper addresses the RF voltages and RF currents of the individual active devices when operating in the circuit. Although performed at small-signal levels, the analysis provides some insight in what causes the power-limiting mechanism when approaching nonlinear conditions.

Finally, the feasibility of the new design method is demonstrated on a 2–26.5-GHz distributed amplifier module employing five discrete GaAs MESFETs. All computations are based on the measured performance characteristics of a representative sample of the transistors used in our experimental amplifiers.

II. The Active Device and Its Model

The characteristics of the active device most commonly expressed by a set of scattering parameters determine its suitability for a particular circuit principle. It therefore seems pertinent to start the discussion with a description of the GaAs MESFET we used in our studies.

The device which has an overall chip size of 0.35×0.35 mm and a gate dimension of 0.25×165 μm is shown in Fig. 1. Its n-type active layer is formed by Si^{29} ion implantation (1.0×10^{13} cm^{-2} at 100 keV). Wafers are annealed at 850°C for 40 min with an As overpressure from an InAs solid source. The peak doping is approximately 4×10^{17} cm^{-3} and the Hall mobility was measured to be 3600 cm^2/V·s at 300°K.

The MESFET quarter micron gates are defined by optical lithography utilizing a controlled erosion, bilayer resist process permitting high yield and excellent uniformity. The

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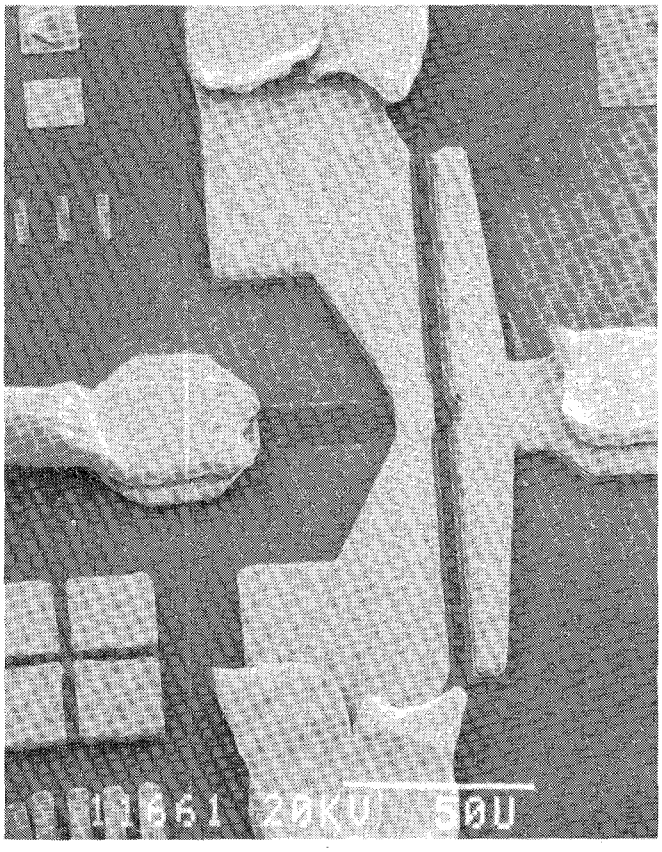


Fig. 1. SEM photo micrograph of the sub-half micron gate GaAs MESFET.

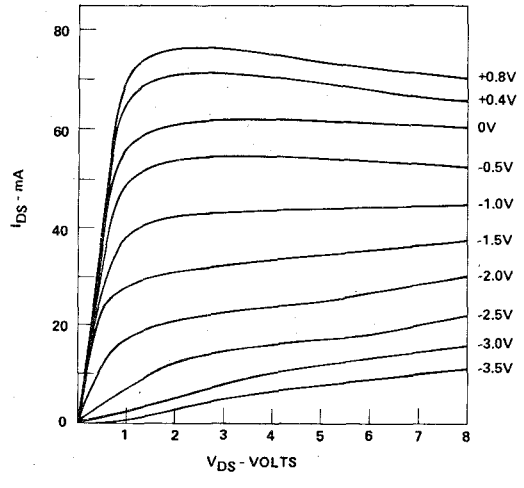
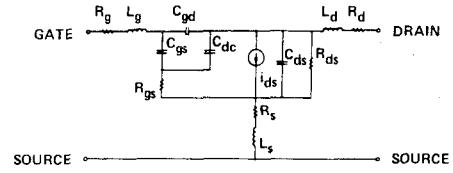


Fig. 2. $I-V$ curves of the GaAs MESFET in Fig. 1.

source resistance (R_s) and the feedback capacitance (C_{dg}) are minimized by angle-evaporating the recessed Al gate toward the source. The ohmic contacts are AuGeNiAu alloyed at 380°C for 30 s and the active region is passivated with a 1000-Å silicon nitride layer. Bonding pads are 3-μm Au plated on top of evaporated Ti/Pt/Au. The device's $I-V$ curves are plotted in Fig. 2.

The typical small-signal gain of the MESFET at $f = 26$ GHz is $G = 10$ dB. The MESFET's model which is based on its S-data measured between 2 GHz and 18 GHz at frequency intervals of 1 GHz is shown in Fig. 3. It has



INTRINSIC ELEMENTS		EXTRINSIC ELEMENTS	
gm = 19 mS		R_g = 2 ohm	
τ_o = 2.4 psec		L_g = .108 nH	
C_{gs} = .15 pF		R_s = .54 ohm	
C_{gd} = .0085 pF		L_s = .052 nH	
C_{dc} = .023 pF		C_{ds} = .010 pF	
R_{gs} = 1.0 ohm		R_d = 1 ohm	
R_{ds} = 430 ohm		L_d = .45 nH	

Fig. 3. Device model based on measured S-parameters.

been assumed to be representative of the transistor's performance to $f = 27$ GHz and was the basis of our computer study. The quality of the model above $f = 18$ GHz has been sufficiently proven by the comparisons made between the computed and the experimental data of our test modules.

III. Comparison of the Computed Performance Parameters

A. The Gain, the Reflection Coefficients, and the Noise Figure

Until very recently, solid-state circuit developers have adhered to the technique of the "identical link" or IL principle when designing distributed amplifier modules; i.e., they have linked the active devices with identical four-ports. While the number of options to optimize the network's performance is somewhat confined, this technique still offers many choices to achieve a desired gain response, evidenced by the excellent results published in the literature [1]–[6]. The only amplifier known to these authors whose design deviates from the IL principle and is based on individual optimization of the linking elements was discussed at the recent Monolithic Circuits Symposium [8]. A typical IL design such as that shown in Fig. 4(a) makes use of circuit elements on the gate side that are different from those employed on the drain side. In addition to its identical gate and drain links, all matching circuits as well as the idle ports' terminations are optimized to achieve a desired gain and VSWR response.

In pursuit of further improvements in electrical performance it seems reasonable to abandon all restrictions including that of the IL design technique and involve all circuit elements in the optimization routine. Such a process guided us to the circuit of Fig. 4(b) which is characterized by drain line elements whose lengths become shorter the closer the link is located towards the output terminal of the gain module. It is for this reason that we have named this new design technique the "declining drain line lengths" or D^2L^2 method. Other characteristic features of the circuit are the capacitive loading which is applied to only two drain terminals of the five MESFETs and the different

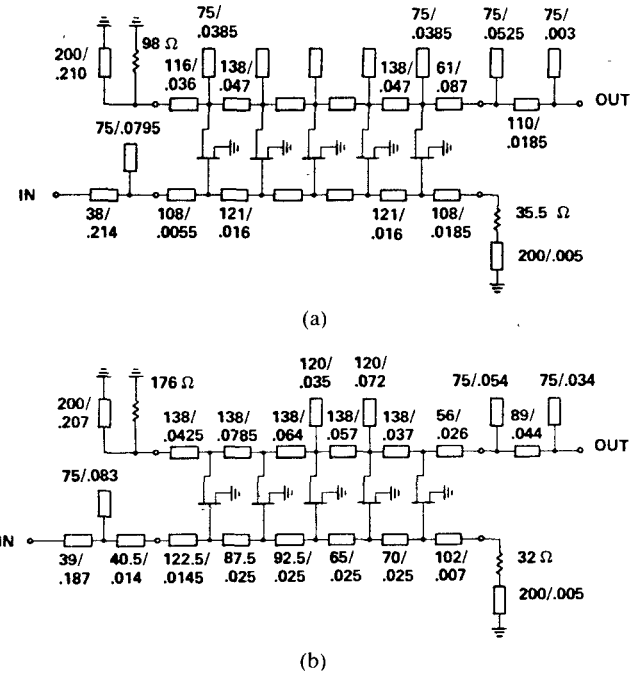


Fig. 4. Schematics of the 2–26.5-GHz amplifier modules based on (a) the "identical links" or IL, and (b) the "declining drain line lengths" or D^2L^2 principle (characteristic impedance in Ω/length in inch for air dielectric).

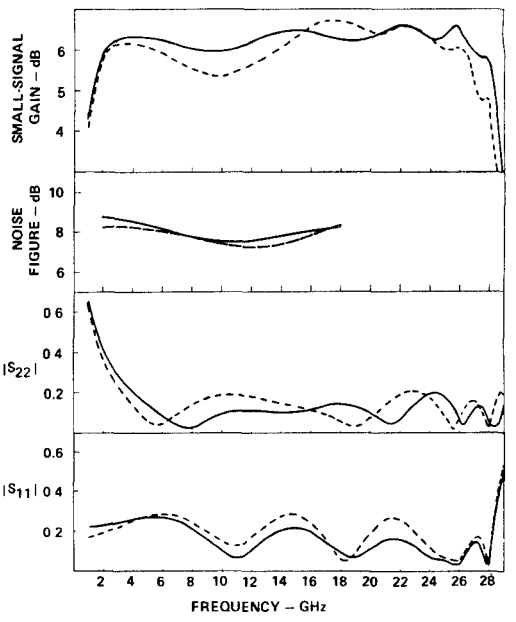


Fig. 5. Comparison of the computed gain (2–29 GHz), noise figure (2–18 GHz), and reflection coefficients (2–29 GHz) of the IL module (dashed curves) and the D^2L^2 module (solid curves).

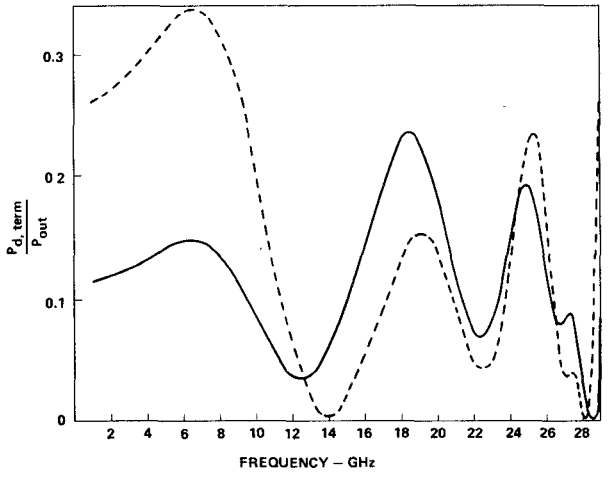


Fig. 6. Ratio of drain termination to output power of the IL module (dashed curve) and the D^2L^2 module (solid curve).

characteristic impedances of the gate transmission lines whose lengths ($l_{air} = 0.025$ in) were kept identical when subjected to the optimization routine. The latter was done in order to attach the transistors at equidistant locations. Both the IL amplifier module and the D^2L^2 amplifier module of Fig. 4 use the device characterized in Fig. 3 and were computer optimized with the same goals and weights. For practical reasons, we imposed a lower and an upper limit on the characteristic impedances of the line elements ($Z_L = 38 - 138$ Ω) corresponding to line widths between 0.033 in and 0.002 in when using 0.010 in thick fused silica as substrate material. The only exception was that made for the drain bias line of $Z_L = 200$ Ω realized with 0.4 mil diameter bond wire. The computed gain and reflection coefficient patterns of the two gain modules are compared in Fig. 5. The curves clearly demonstrate the improved gain flatness and extended frequency coverage which was obtained with the D^2L^2 circuit without impairing either the input or the output reflection coefficient.

When covering a frequency band as wide as 2 GHz to 27 GHz, obviously not all of the power amplified by the FETs is delivered to the output load. A fraction of the power is dissipated in the drain termination. Fig. 6 compares the ratio of the power dissipated by the drain termination resistor to that forwarded to the output load. While there are portions of the frequency band in which the D^2L^2 termination absorbs more power than the IL termination, its power dissipation when averaged over the entire frequency band is clearly superior.

There is another important benefit offered by the D^2L^2 distrubuted amplifier. When using discrete devices as is the case in hybrid circuits, the IL design method may encounter a dimensional problem tied to the width of the active device. For example, in case of the IL module in Fig. 4(a), the physical width of the device (Fig. 1) exceeds the optimum length of the gate line element even when realized on 0.010 in thick fused silica ($l_{diel} = 0.010$ in for $l_{air} = 0.016$ in) by 0.004 in. Hence the width of the device ($w = 0.014$ in) requires a minimum line length of $l_{diel} = 0.015$ in to accommodate the FETs. In contrast, the D^2L^2 module of Fig. 4(b) calls for an optimum gate line length of $l_{air} = 0.025$ in corresponding to approximately $l_{diel} = 0.015$ in on the same substrate material for the range of the characteristic impedances indicated.

Even though the amplifiers of Fig. 4 were optimized for gain, gain flatness and VSWR only, it is of some interest to compare their computed noise behavior. Unfortunately, this part of our studies is limited to the 2–18-GHz frequency band for we were unable to measure the devices's noise

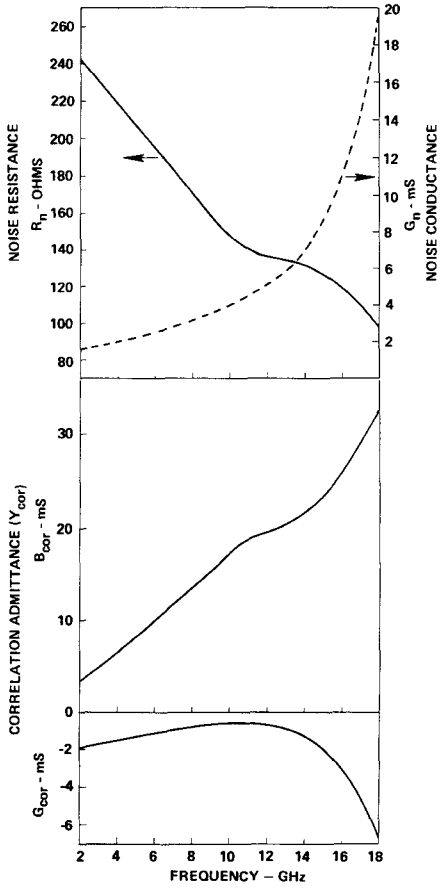


Fig. 7. Characteristic noise parameters of the GaAs MESFET in Fig. 1 measured between 2 GHz and 18 GHz.

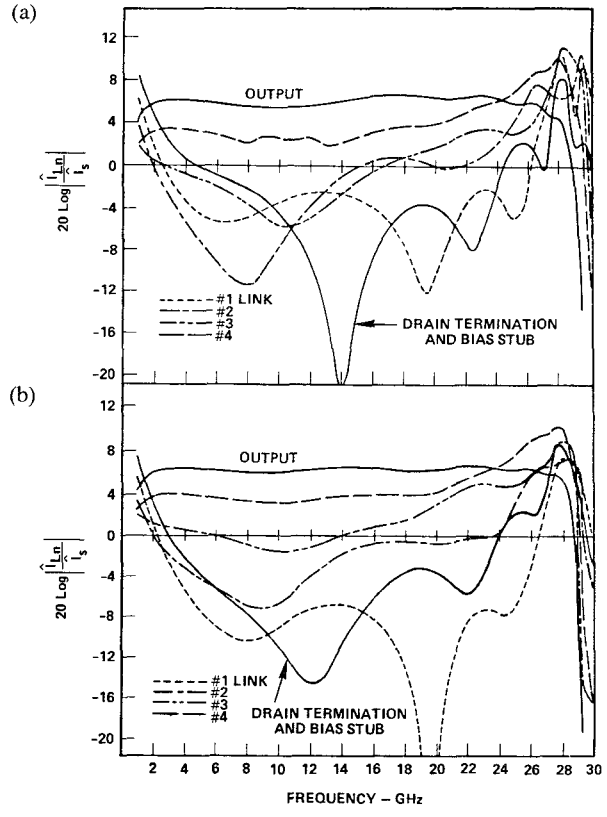


Fig. 8. Relative RF current amplitudes in the drain line of (a) the IL module, and (b) the D^2L^2 module.

parameters above 18 GHz with the accuracy required for such an investigation. The results of our efforts are reflected in the noise parameters of Fig. 7 which were computed from the measured data of the noise figure, the minimum noise figure and its optimum source impedance. Based on these noise parameters we were able to compute the noise figure of the IL and the D^2L^2 gain modules of Fig. 4 using a program described in the literature [9]. The results are also presented in Fig. 5 which, in addition to the gain and the reflection coefficients, shows the noise figure curves of both circuits between 2 GHz and 18 GHz. From the data displayed, it is clearly evident that the noise figure of the IL circuit has a slight advantage across the 2–18-GHz frequency band. However, due to the better gain characteristics of the D^2L^2 module above 24 GHz, there is a reasonable doubt that the advantage will hold up in *K*-band.

Now that we have compared the performance of the circuits in Fig. 4, we will briefly take a look at the possible reasons for the better gain flatness and wider bandwidth displayed by our D^2L^2 circuits. Obviously, our MESFET is characterized by input and output admittances that deviate significantly from the capacitive shunts that are required to form artificial transmission lines. Furthermore, the gate line and the drain line are coupled with each other by the devices' feedback elements (C_{ds}, C_{dc}, R_s, and L_s) adding to the already complicated task to terminate the lines with a minimum buildup of standing waves. And finally, from computer studies we have learned that optimum gain and VSWR performance requires termination resistors other than those equal to the characteristic impedances of the idealized artificial transmission lines. As a result, the drain ports of the individual devices are no longer terminated by identical impedances and synchronism between the voltage waves in the gate and the drain line cannot be maintained. It can be shown that the deviation from synchronism in an IL circuit may be significantly reduced by successively decreasing the lengths of the drain links. For example, the maximum deviation from synchronism (expressed in phase length) occurring between 2 GHz and 27 GHz was reduced from $\Delta\varphi_{max} = 97°$ in the IL circuit of Fig. 4(a) to $\Delta\varphi_{max} = 50°$ in the D^2L^2 circuit of Fig. 4(b). The average phase deviation of all FETs in the same band is $\Delta\varphi_{av} = 29°$ in the case of the IL unit versus $\Delta\varphi_{av} = 19.5°$ in the case of the D^2L^2 unit. Furthermore, since the output power is composed of the currents of the individual active devices, we may find an additional clue by analyzing the amplitudes of the currents flowing in the links. This is done in Fig. 8 which shows the relative amplitudes of the output current, the four drain link currents and the termination resistor-bias stub network current. All results are referenced to the amplitudes of the source voltage $\hat{V}_s$ and the source current $\hat{I}_s$; i.e., for the case that the load is matched to the 50-Ω source impedance. It is evident from these plots that the buildup of the current amplitudes has a less periodical character in case of the D^2L^2 circuit and consequently results in the smoother output current and gain. In addition, the D^2L^2 circuit's less complicated current pattern at frequencies above 26 GHz seems to be responsible for this concept's slightly wider bandwidth. In short, the phase

correction provided by the D^2L^2 concept improves the phase conditions between the voltage of the gate and drain line and smooths out the amplitudes of the currents flowing in the drain links.

B. Voltages and Currents of the Active Devices

As discussed earlier, the output power of the distributed amplifier stage is composed of the contributions of several transistors whose RF currents are superimposed in the drain line. Hence, the module's gain depends greatly on the amplitude and the phase conditions of the RF drain currents and RF drain voltages relative to each other. The ideal amplifier adds up the active device's power contributions in such a way that almost all power appears at the output and none at the drain termination. However, these conditions can only be approached under hypothetical conditions not compatible with practical active devices. As has been demonstrated in Fig. 6, noticeable amounts of power reach the drain terminal when GaAs MESFETs are used in multi-octave amplifiers even when designed for optimum performance. Since the results of Fig. 6 suggest that the superposition of the MESFETs' contributions to the output power are far from ideal, their RF voltages and RF currents must significantly differ from each other in both amplitude and phase. Hence, the questions arise which of the FETs is burdened the most regarding its voltage and/or current limits and what portions of the frequency band put the heaviest load on the devices. Once the answers are known, circuit techniques may be devised that provide a more even distribution of the RF currents and/or voltages among the transistors. The design of a 2–8-GHz power amplifier in which the attempt was made to equalize the RF gate voltages by means of capacitive voltage dividers has been reported [10]. The authors also, in passing, propose the concept of the decreasing drain-line lengths, however, for an entirely different purpose. The use of decreasing drain-line and gate-line lengths is suggested to correct for the phase differences across each cell due to the graded profile of the gate capacitors.

While an exact study of the devices under nonlinear operating conditions requires the use of a large-signal analysis, we will resort to the much less complicated small-signal computations since our interest is mostly of a qualitative nature. Due to the latter, the valid assumption is made that those devices that carry the heaviest voltage or current burden under small-signal operating conditions approach power-limiting conditions before their neighbors do. Using this reasoning, we expect the simplified analysis to indicate those portions of the frequency band in which nonlinear operation is likely to occur first. Beyond that, the evaluation is performed to broaden our understanding of the additive amplification process in distributed amplifiers.

The relative RF voltage and RF current amplitudes of each MESFET for both the IL and the D^2L^2 module (Fig. 4), are plotted in Fig. 9 and Fig. 10, respectively. From either set of curves, it becomes immediately evident that the relationship between the respective RF-parameters of the individual transistors is of a very complex nature. An increase of both the RF-drain voltage and RF-drain current amplitudes towards the high end of the frequency

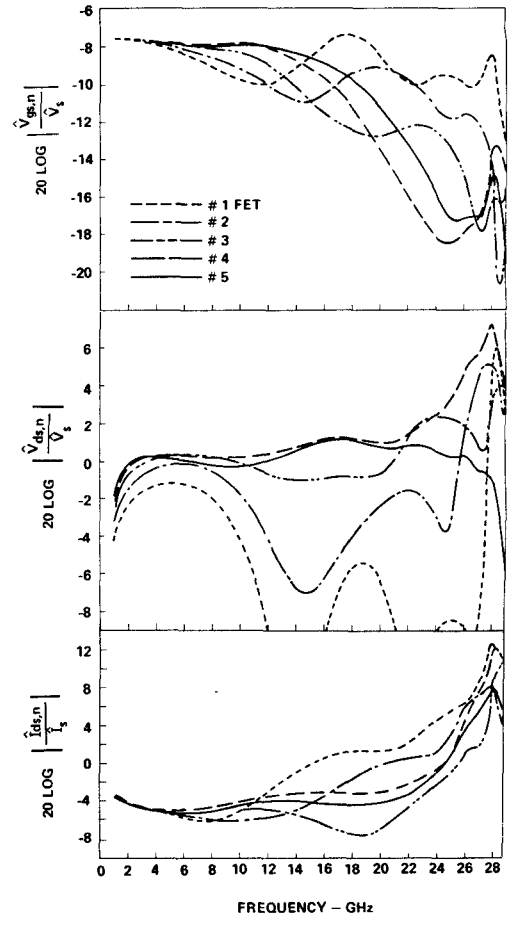


Fig. 9. Relative RF voltage and current amplitudes of the individual transistors for the IL module.

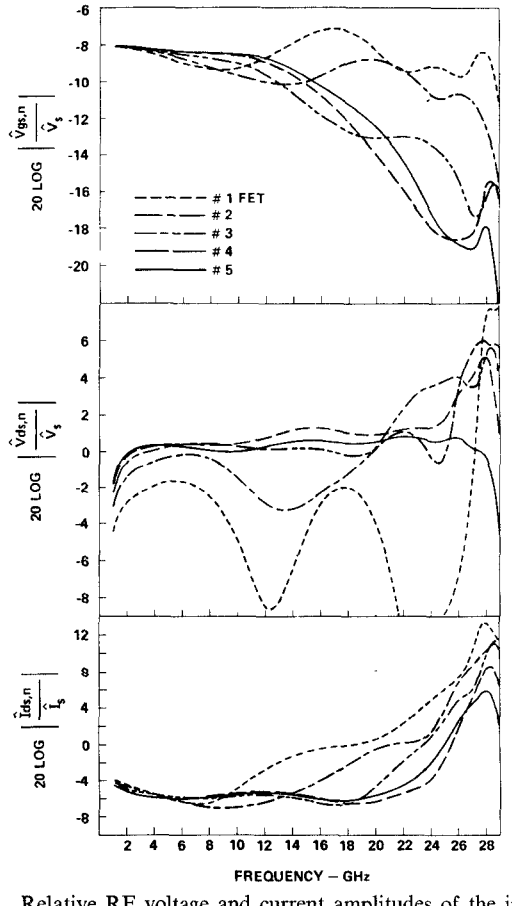


Fig. 10. Relative RF voltage and current amplitudes of the individual transistors for the D^2L^2 module.

band is also easily discernible, suggesting that nonlinear operation is first approached at high frequencies. Below $f = 8$ GHz, all devices may be considered as essentially carrying equal voltage and current loads except for the MESFET closest to the input (FET #1) which has a comparatively lower RF-drain voltage. However, from $f =$ 10 GHz (D^2L^2) and $f = 12$ GHz (IL), respectively, to $f = 27$ GHz, the first transistor displays the highest RF-drain current while its RF-drain voltage remains below those of its neighbors. Except for the lower half of the frequency band, the input MESFET is exposed to the highest RF-gate voltage.

Let us now attempt to draw some qualitative conclusions from our small-signal computations. On account of the preceding analysis we expect nonlinear operation in our two amplifiers to occur first at the upper end of the frequency band. With increasing drive level, it is anticipated to progress towards lower frequencies. However, the curves of the relative RF drain voltage amplitudes of Fig. 9 and Fig. 10 suggest that below approximately $f = 20$ GHz, the unit's gain compression becomes nearly independent of frequency if the RF drain voltage is the parameter responsible for limiting the output power. On the other hand, the band in which the compression is independent of frequency, is shifted to frequencies below approximately $f = 10$ GHz if the RF drain current is the responsible force. Hence, the question arises which of the two RF paramters, drain voltage or drain current, dominates the gain module's characteristics when approaching large-signal operation. Both, of course, are controlled by the RF gate voltage.

In order to find the parameter or parameters that cause the nonlinear operation of our D^2L^2 amplifier stage, we first measured the input power required to compress its gain by 1 dB (Fig. 11) and then drew on the small-signal parameters of Fig. 10 to determine the unit's approximate RF gate voltage, RF drain voltage, and RF drain current amplitudes. The measurements were performed on an experimental D^2L^2 module whose circuit is represented in the schematic of Fig. 4(b) and briefly described in Section IV. Obviously, due to the fact that the amplifier is operating under nonlinear conditions, the following analysis is of rather qualitative nature. A method to much more accurately predict the nonlinear performance of GaAs MESFET devices utilizing time domain analysis and experimentally characterized bias dependence of device model elements has been reported in the literature [11]. However, the attempt to decide upon the cause of the gain compression in our D^2L^2 module at the 1-dB compression level with the proposed simplified method leads to sensible results.

Fig. 12 shows the RF voltage and current amplitudes as derived from the measured source voltage amplitude $\hat{V}_s$, the measured source current amplitude $\hat{I}_s$, and the computed curves of Fig. 10. The bias conditions of the experimental module were $V_{DS} = 4$ V, $V_{GS} = -1.25$ V, and $I_{DS} =$ 39 mA per FET. Consulting the MESFET's I–V curves in Fig. 2, we then expect nonlinearities to appear at approximately $\hat{V}_{ds} > 2.8$ V, $\hat{V}_{gs} > 1.25$ V, and $\hat{I}_{ds} > 25$ mA. Using these quantities as guidelines and comparing them

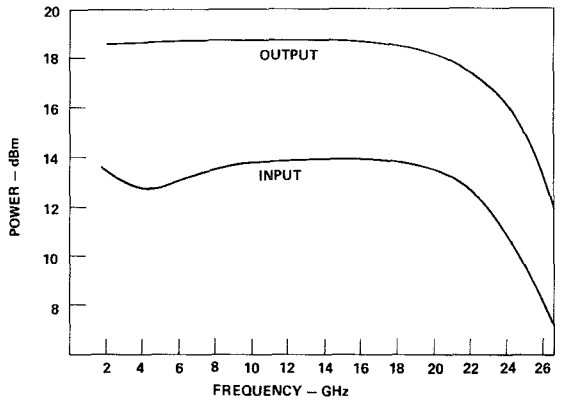


Fig. 11. Measured RF output powers of the D^2L^2 amplifier module at the indicated input powers for $V_{GS} = -1.25$ V and $V_{DS} = 4$ V (1-dB compression).

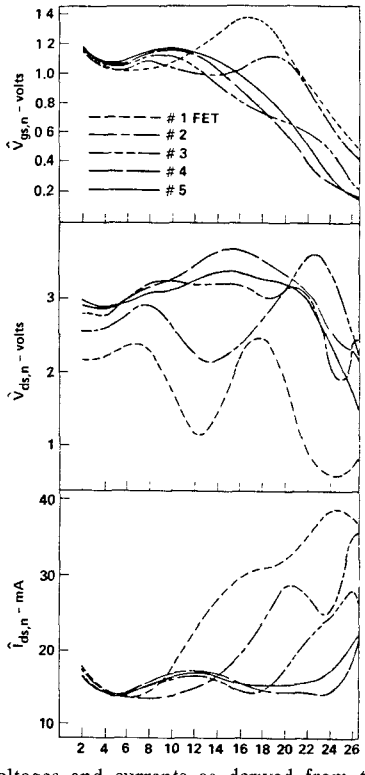


Fig. 12. RF voltages and currents as derived from the signal source power necessary to drive the D^2L^2 module at its 1-dB gain compression point and the computed curves of Fig. 11.

with the RF parameters plotted in Fig. 12, it appears that up to $f = 10$ GHz the RF drain current is clearly not limiting the output power. Drain current limited operation occurs above $f = 13$ GHz for the device closest to the input (FET #1) while for FET's #2 and #3 it is found above $f = 18$ GHz and $f = 24$ GHz, respectively. Up to at least $f = 22$ GHz, the majority of the transistors (FET's #3, #4, and #5) are operating drain voltage limited.

In summary, the qualitative study reveals that gain compression of our D^2L^2 module over the lower 90 percent of the frequency band is dominated by drain voltage limiting while over only the last 10 percent of the band it seems to be primarily caused by drain current limited operation. The results in the lower 45 percent and upper 5 percent

band in regard to the cause of the gain compression are quite distinct, leaving a 50 percent range in which both effects are present, however, with drain voltage limiting as the dominating component.

IV. The Amplifier and Its Performance

The experimental D^2L^2 amplifier module was realized on 0.010 in thick fused silica in accordance with the schematic of Fig. 4(b). The five GaAs MESFETs were located side by side on a copper rib separated by 2-mil gaps to allow for grounding the source of each device by means of a wire mesh ribbon. Ultimately, this technique will be replaced by inserting a single bank of five MESFETs whose sources are grounded through via holes. The termination resistors in the gate and the drain line were etched into a tantalum nitride film which was deposited below the thin gold film that makes up the conducting circuit elements. As shown in Fig. 4(b), biasing was provided through the drain and gate short circuit shunt stubs avoiding any dc power dissipation. A photograph of the module is presented in Fig. 13.

At first turn-on, the untuned module displayed a flat gain performance of $G = 5.1 \pm 0.6$ dB between 2.0 GHz and 24.5 GHz and surprisingly little effort was necessary to improve the gain to that shown in Fig. 14 of $G = 6.1 \pm 0.6$ dB from 2.0 GHz to 26.5 GHz. In fact, modifications to the circuit represented in Fig. 4(b) by tuning were made almost exclusively to the input and output matching network. The module's maximum input and output reflection coefficients were $|S_{11}| = 0.45$ and $|S_{22}| = 0.4$, respectively, despite the chosen high efficiency biasing scheme. Noise figures of the module ranged from a maximum of 9.9 dB to a minimum of 7.9 dB across the 24.5-GHz band. As displayed in Fig. 11, the unit's 1-dB compression output power remained between 18.0 and 18.8 dBm from 2 GHz to 20 GHz and dropped, however, to 12.0 dBm at 26.5 GHz due to the reasons discussed in the preceding section.

The experimental proof of the theoretical results as to the causes of nonlinear operation, i.e., voltage and/or current limiting is a rather difficult task. For example, an increase of the drain source voltage (V_{DS}) at constant input power decreases the ratio of the RF to d.c. voltages at the drain terminals of the MESFETs but, unfortunately, also changes the gain of the devices and increases their operating temperatures. In addition, each of the five transistors faces a different load impedance that due to the other four devices is dependent on the bias conditions. A simple experiment, then, in which we alter the drain source voltage can provide us only with approximate answers. In Fig. 15, we have plotted for each frequency the RF power gained when the experimental amplifier module was operated at the 1-dB compression point for $V_{DS} = 4$ V ($V_{GS} = -1.25$ V) and, at this input power level, the drain-source voltage was raised to $V_{DS} = 5$ V. In order to achieve meaningful results, a correction of the data to allow for the change in gain due to the increase in the drain bias voltage was made. The resulting curve shows a rise, though lower than expected, in output power. Furthermore, it exhibits a

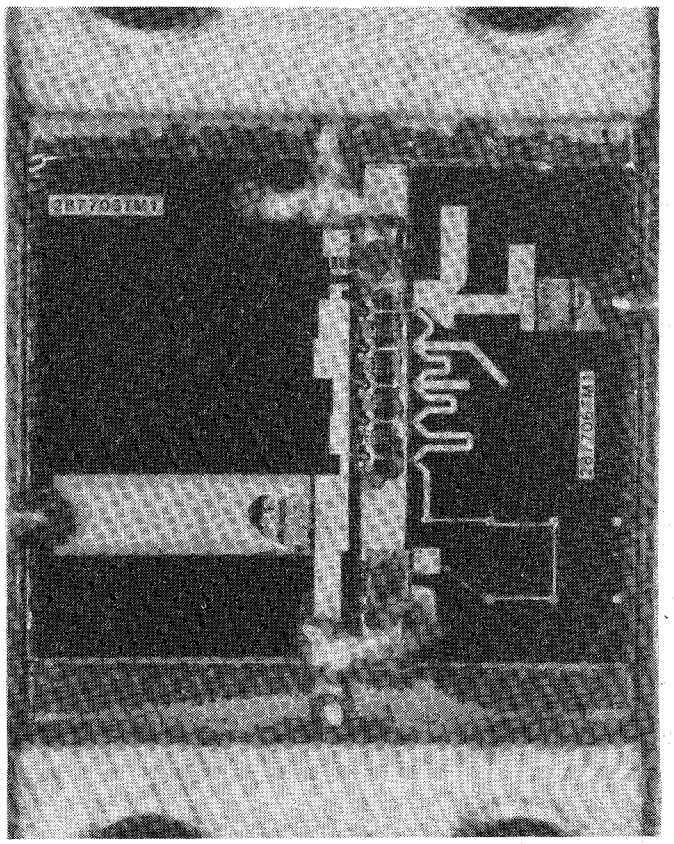


Fig. 13. Photograph of the D^2L^2 amplifier module.

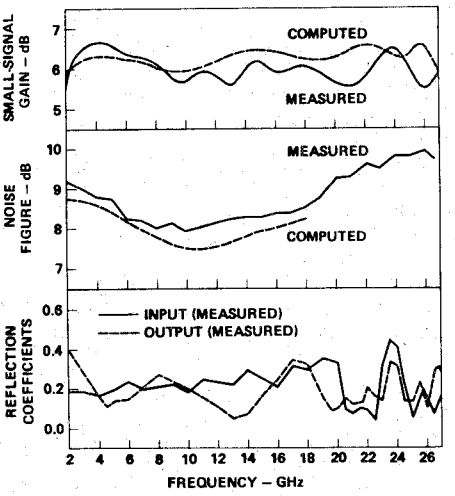


Fig. 14. Measured and computed small-signal gain, noise figure, and reflection coefficients of the 2–26.5-GHz D^2L^2 amplifier module.

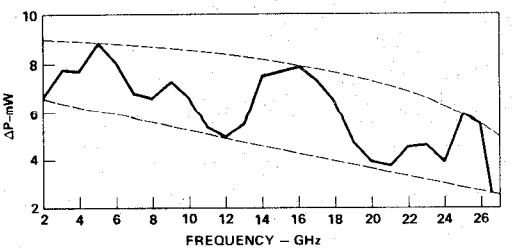


Fig. 15. Gained output power due to an increase in drain bias voltage from $V_{DS} = 4$ V to $V_{DS} = 5$ V at the input power levels shown in Fig. 11.

progressively declining trend in the gained output power with frequency indicating thet the influence of RF drain voltage limiting decreases with frequency.

V. Summary

The computed performance parameters of the "declining drain line lengths" circuit and the "identical links" circuit have been compared. It was shown that for a given GaAs MESFET, the D^2L^2 design outperformed the IL design in the areas of gain flatness and bandwidth. The improvement is believed to be due to the more synchronous phase conditions between the RF gate the RF drain voltages of the D^2L^2 circuit, resulting in a smoother pattern of the individual drain link currents. By means of the small-signal computations of the relative RF drain voltages and currents and the measurements of a D^2L^2 amplifier's input power, an attempt has been made to find a qualitatve answer as to the causes of the power limiting effects at the 1-dB compression points. It was found that nonlinear operation at the lower frequencies is caused by voltage limiting, while at the very high end of the frequency band it is brought about by current limiting effects. Finally, the measurements of gain, VSWR, noise figure and output power performed on an experimental 2–26.5-GHz amplifier are discussed and, expect for the last parameter, compared with the computed data. The measured results are in good agreement with the theoretical predictions and are very encouraging in regard to the future of the D^2L^2 circuit.

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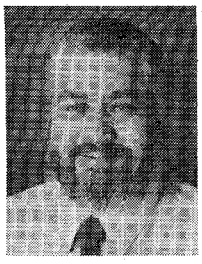

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